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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,144	10/19/2001	Hideo Nakagawa	740819-673	7544

22204 7590 07/13/2004

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EXAMINER	
ANDUJAR, LEONARDO	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,144	NAKAGAWA ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-15* is/are pending in the application.

4a) Of the above claim(s) *8-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The amendment filed on 04/20/2004in response to the Office action mailed on 01/21/2004 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-11 and 13-15

Election/Restrictions

2. Applicant's election without traverse of Group I (claims 1-7) in Paper No. 5 is acknowledged.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Initially, and with respect to claims 1, 2, 4 and 15, note that a "product by process" claim is directed to the product per se, no matter how actually made. See In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the

process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); Buono v. Yankee Maid Dress Corp., 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935). Note that Applicant has the burden of proof in such cases as the above case law makes clear.

5. Claims 1-7 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6,303,498) in view of Admitted Prior Art (hereafter APA).

6. Regarding claim 1, Chen (e.g. figs. 3b/c) shows most aspects of the instant invention including a semiconductor device comprising: a metal interconnect made from a multi layer film composed of a first metal film 11 deposited on a semiconductor substrate; a second metal film 28 which is a seed layer deposited on the first metal film; a an interlayer insulating film 14 formed on the second metal film; a via hole 18 formed in the interlayer insulating and for exposing the second metal film; and a plug 32 made from a third metal film formed on the second metal film that is exposed at the bottom of the via hole. Also, the seed layer is laminated on the first metal film.

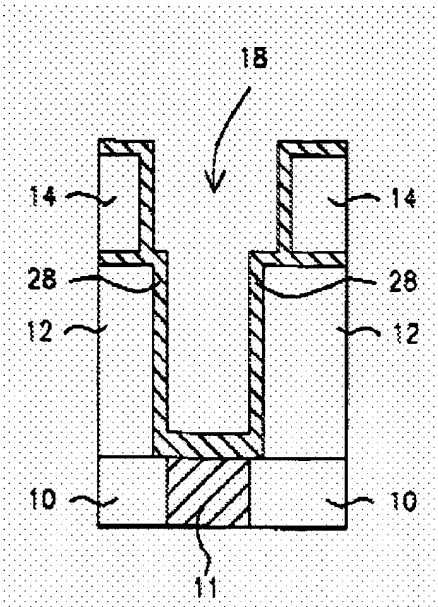

FIG. 3b

In regards to the method for forming the third metal film, it is noted that selectively growing is an intermediate process step that does not affect the structure of the final device. Chen does not explicitly depict an insulating film sandwiched between the first metal film and the substrate. Nonetheless, Chen implicitly teaches this limitation since the metal film 11 is part of a multilevel interconnection (col. 3/lls. 61-66). As it is well known the art a multilevel interconnection includes one or more insulating films sandwiched between the metal films and the substrate (see for example applicant admitted prior art fig. 17A). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an insulating film sandwiched between the first metal film and the substrate to isolate the first metal film from the substrate or from any electronic component formed in the substrate surface.

7. Regarding claim 2, Chen shows a third metal film. In regards to the method for forming the third metal film, it is noted that plating is an intermediate process step that does not affect the structure of the final device.

8. Regarding claim 3, Chen discloses that the second metal film and the third metal film are both made of copper (col. 5/lls. 41-50).

9. Regarding claim 4, Chen teaches that the second metal film and the third metal film are made from a metal including copper as a principal constituent (col. (col. 5/lls. 41-50). Chen does not show the use of an adhesive between the metal interconnects (e.g. fig. 3b). In regards to the method for forming the third metal film, it is noted that plating is an intermediate process step that does not affect the structure of the final device.

10. Regarding claim 5, APA (e.g. fig. 20B) shows an air gap 24 formed between the metal interconnects in the insulating film.

11. Regarding claim 6, Chen in view of APA shows a first and second metal, which inherently have resistance values. Chen in view of APA does not explicitly teach the resistant ratio of the interconnection layers. Nonetheless, it well known in the art those resistance ratios of the interconnection layers are subject to optimization. For example, US 6,136,707 teaches that the requirement for providing a low resistance electrical path is fulfilled by choosing the seed layer to be comprised of an adequately thick, low resistivity material (col. 1/lls. 33-36). In this case, the specific ratio claimed by applicant, i.e., "wherein said first metal film composing said metal interconnect has interconnect resistant substantially 1/5 /or less of interconnect resistance of said second metal film composing said metal

interconnects", absent any criticality, is only considered to be the "optimum" resistant ratio of the metal interconnect layers disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, low resistance electrical path, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as the interconnection is used as already suggested by the Prior Art.

12. Regarding claim 7, Chen in view of APA shows a first and second metal, which inherently have resistance values. Chen in view of APA does not explicitly teach the resistance of the first metal layer is substantially equivalent to the resistance of the second layer. Nonetheless, it well known in the art that the resistance ratio of the interconnection layers is subject to optimization. For example, US 6,136,707 teaches that the requirement for providing a low resistance electrical path is fulfilled by choosing the seed layer to be comprised of an adequately thick, low resistivity material (col. 1/lls. 33-36). In this case, the specific resistance claimed by applicant, i.e., "wherein said first metal film composing said metal interconnect has interconnect resistant substantially equivalent to interconnect resistance of said second metal film composing said metal interconnects", absent any criticality, is only considered to be the "optimum" resistant ratio of the metal interconnect layers disclosed by the Prior Art that a person having ordinary skill in the art would have been able to

determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, low resistance electrical path, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as the interconnection is used as already suggested by the Prior Art.

13. Regarding claim 13, APA (e.g. fig. 20B) shows that the width of the air gap 24 is substantially equal to the space between the metal interconnects.

14. Regarding claim 14, Chen shows that the layer is formed over the entire surface of the first metal film.

15. Regarding claim 15, Chen (e.g. figs. 3b/c) shows most aspects of the instant invention including a semiconductor device comprising: a plurality of metal interconnects made from a multi layer film composed of a plurality of first metal films 11 deposited on a semiconductor substrate; a plurality of second metal films 28, which are seed layers, deposited on the plurality of first metal films; an interlayer insulating film 14 formed on the plurality of second metal films; a plurality of via holes 18 formed in the interlayer insulating and for exposing the plurality of second metal films; and a plurality of plugs 32 made from a third metal film formed on the plurality of second metal films that are exposed at the bottom of the plurality of via holes. Also, the seed layers are laminated on the first metal films. Although not depicted, Chen invention includes a plurality of interconnections such as that depicted in figure 3 because this structure is part of an interconnection network (col. 3/lls. 61-66).

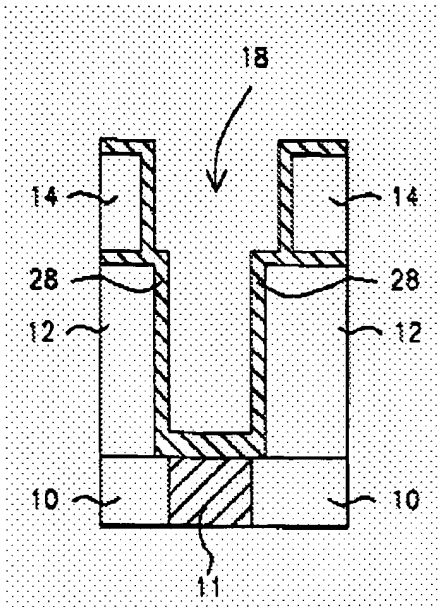

FIG. 3b

In regards to the method for forming the plurality of third metals film, it is noted that selectively growing is an intermediate process step that does not affect the structure of the final device. Chen does not explicitly depict an insulating film sandwiched between the plurality of first metal films and the substrate. Nonetheless, Chen implicitly teaches this limitation since the plurality of metal films 11 are part of a multilevel interconnection (col. 3/lls. 61-66). As it is well known the art a multilevel interconnection includes one or more insulating films sandwiched between the metal films and the substrate (see for example applicant admitted prior art fig. 17A). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an insulating film sandwiched between the plurality of first metal films and the substrate to isolate the plurality of first metal films from the substrate or from any electronic component formed in the substrate surface.

Response to Arguments

16. Applicant's arguments with respect to claims 1-7 and 14-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The

fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 257/678, 773, 774, 775; 438/618, 622,625	07/04
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	07/04

Leonardo Andújar
Patent Examiner Art Unit 2826
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07/01/2004

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